IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
VINSON ET AL.

Serial No. **10/696,918**

Filing Date: **October 30, 2003**

Confirmation No. **8239**

For: **DECOUPLING CAPACITOR CLOSELY COUPLED WITH INTEGRATED CIRCUIT**

Examiner: T. Tran

Art Unit: 2822

DECLARATION UNDER 37 CFR SECTION 1.131

Mail Stop Amendment
Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

Sir:

We, **Robert S. VINSON, Joseph B. BRIEF, Donald J. BECK, and Gregory M. JANDZIO,** hereby declare:

1. We are the co-inventors of the subject matter of the above-identified patent application.

2. We conceived of the subject matter of the above-identified patent application while working in our laboratories in the United States at Harris Corporation in Palm Bay, Florida prior to July 12, 2000, the effective date of U.S. Patent No. 6,429,536 to Liu et al.

3. We conceived of an integrated circuit chip module that would have improved decoupling capacitor characteristics with decreased equivalent series inductance

and equivalent series resistance. We worked diligently from conception before July 12, 2000 to reduction to practice on August 22, 2000 of an integrated circuit chip module that includes a substrate, integrated circuit die mounted on the substrate and having die pads and an exposed surface opposite from the substrate. A plurality of substrate bonding pads are positioned on the substrate adjacent the integrated circuit die. A decoupling capacitor assembly is mounted on the integrated circuit die and includes a capacitor carrier secured onto the exposed surface of the integrated circuit die, the decoupling capacitor, thin film metallization layer and conductive adhesive layer engaging the decoupling capacitor and thin film metallization layer and securing the decoupling capacitor to the capacitor carrier. In some aspects, the wire bond extends from a thin film metallization layer to a logic pin on the integrated circuit die and from a logic pin to a substrate bonding pad. A plurality of decoupling capacitor assemblies can be mounted on the integrated circuit die and is shown in FIG. 2 of the patent application. A number of the IC's and associated components can be positioned on the substrate.

4. Exhibits 1 and 2 are photographs of the reduced to practice module. Exhibit 1 includes a top plan view and a side elevation view showing a decoupling capacitor assembly that includes the capacitor carrier, decoupling capacitor, and

wire bonds. Exhibit 2 is a side elevation view showing a capacitor, a metallized thin film as a metallized carrier, the carrier, and die.

5. After reducing to practice the invention on August 22, 2000, we worked to improve the invention and filed a patent application on our invention.

6. We hereby declare that all statements made herein of our own knowledge are true, and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements, and the like so made, are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Sept 6, 2005
Date

ROBERT S. VINSON

9/15/05
Date

JOSEPH B. BRIEF

Date

DONALD J. BECK

9-6-2005
Date

GREGORY M. JANDZIO

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Date — ROBERT S. VINSON

Date — JOSEPH B. BRIEF

10/3/05
Date — DONALD J. BECK

Date — GREGORY M. JANDZIO